**ECE522 - CMOS INTEGRATED CIRCUITS Ⅰ**

FINAL PROJECT

by

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## **PROJECT AIM**

The aim of the project is to design a two stage single ended CMOS Op-Amp with Miller (pole splitting) compensation in the 0.18 um process. The parameters for this process were provided on Canvas. The specifications needed to be met were as follows.

|  |  |
| --- | --- |
| Load Capacitance | 5pF |
| Power Supply | Vdd = 0.9V, Vss = -0.9V |
| Open loop gain | ≥ 65 dB |
| Phase Margin | ≥60° |
| Unity Gain Frequency | ≥ 15 MHz |

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## **SCHEMATICS WITH EXPLANATION**

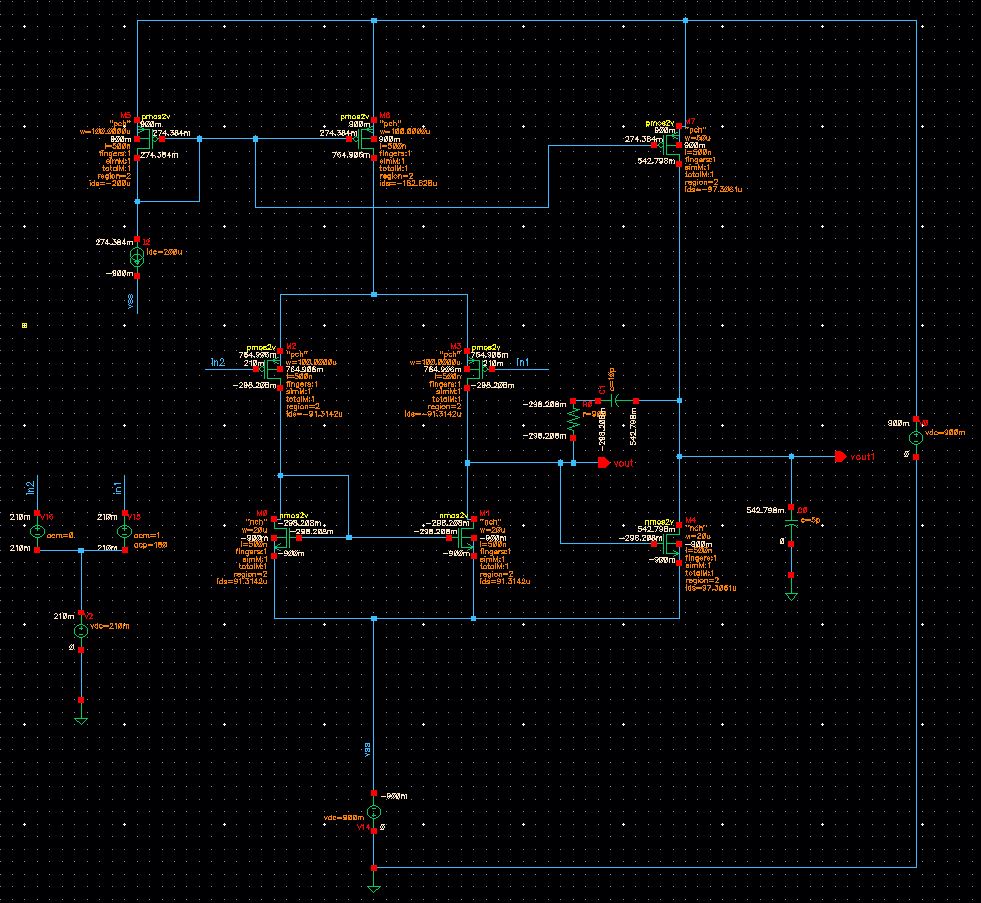


Figure-1

We are using the figure-1 schematics for our project which is two stage opamp with a differential input and single ended output. We are using current mirror circuit for biasing. An ideal current source is used in the current mirror which is of 200uA. For our schematics vdd is +0.9V and Vss is -0.9V as required for project. We are also using the miller compensation between two stages for pole splitting.

Following is the expression used for calculating gain.

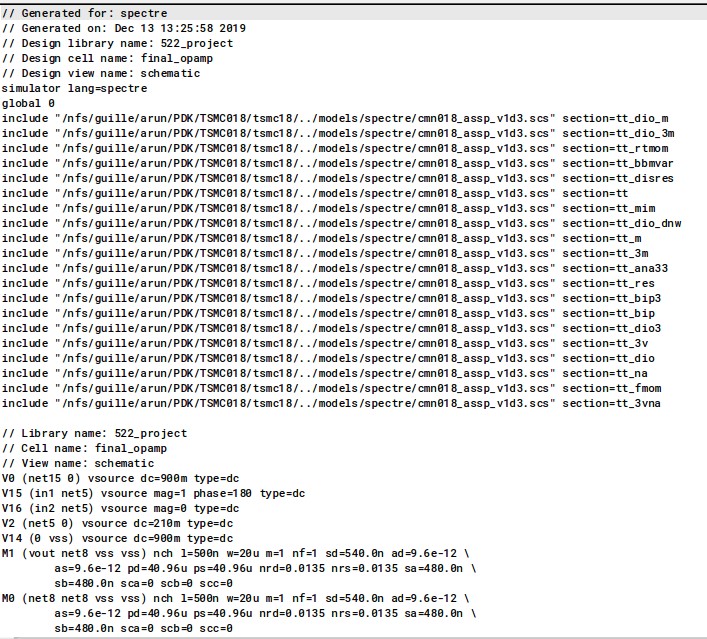
Gain = gm2\*(rds3||rds1) \* gm4\*(rds4||rds7)

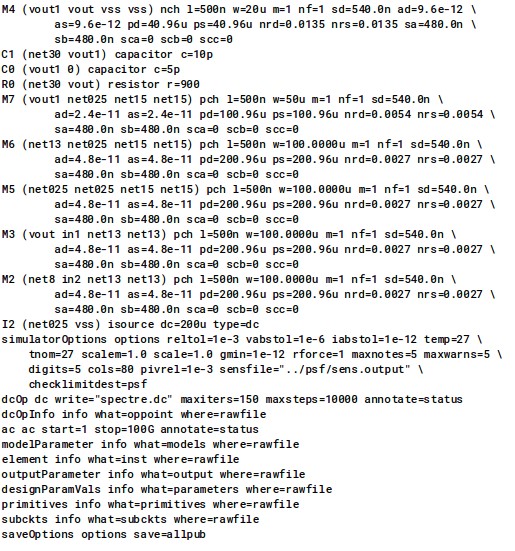
gm2\*(rds3||rds1) is the gain of first stage and gm4\*(rds4||rds7) is the gain of second stage. As we can see that gain depends mainly on two things, one is gm of input transistor and second is rds of output transistors. So we kept the width of input transistors high to get high gm and then we increased length of transistors to 500nm to increase the rds of transistors which helped us to achieve the required gain. We are using compensation capacitor of 10pF and resistor of 900 ohms for pole splitting. Following table shows the sizes of all the transistors used in the schematics.

**SIZES OF THE TRANSISTORS**

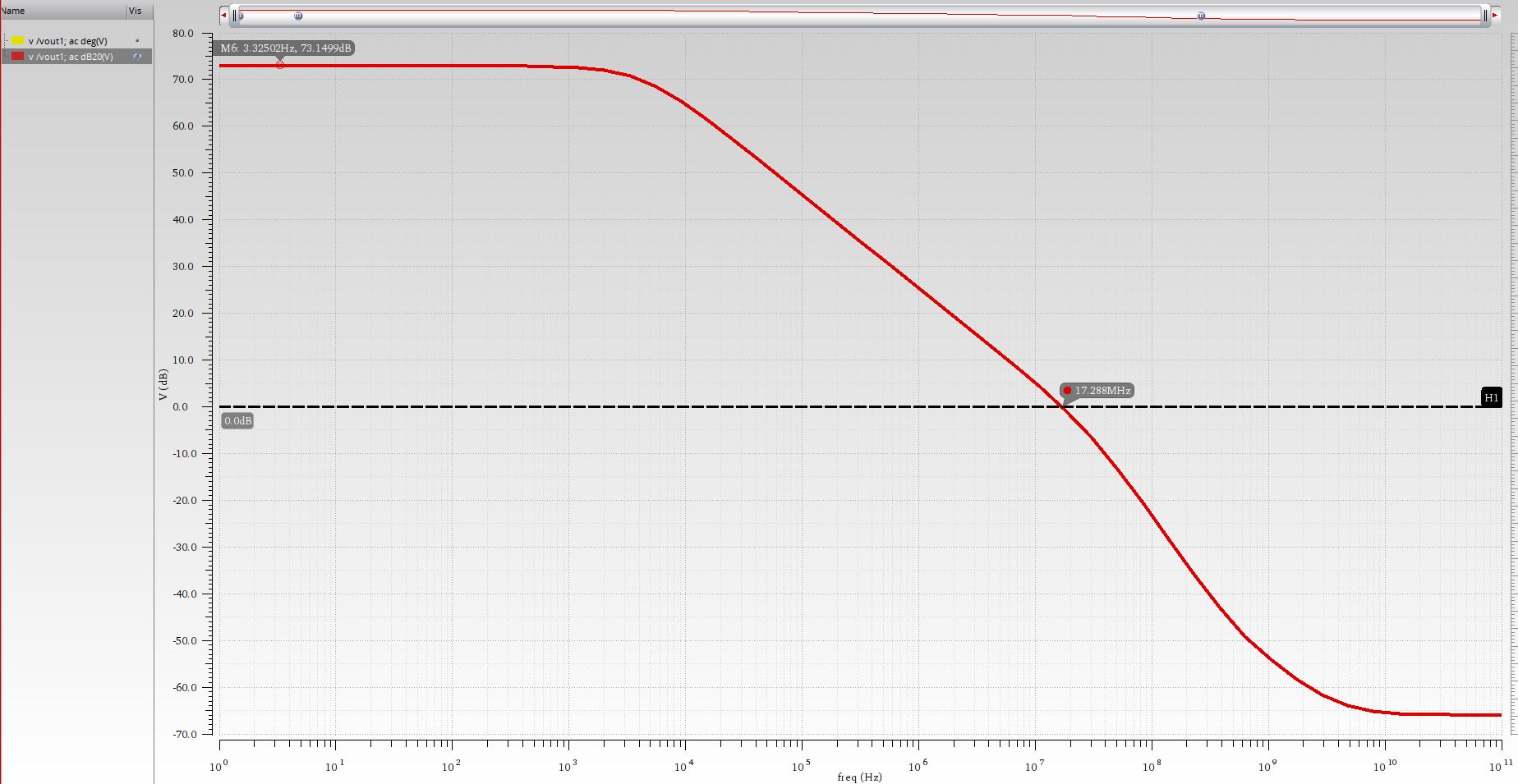
|  |  |  |
| --- | --- | --- |
| **MOSFETS** | **WIDTH (W)** | **LENGTH (L)** |
|  |  |  |
| M0 | 20u | 500n |
| M1 | 20u | 500n |
| M2 | 100u | 500n |
| M3 | 100u | 500n |
| M4 | 20u | 500n |
| M5 | 100u | 500n |
| M6 | 100u | 500n |
| M7 | 50u | 500n |

**NETLIST**

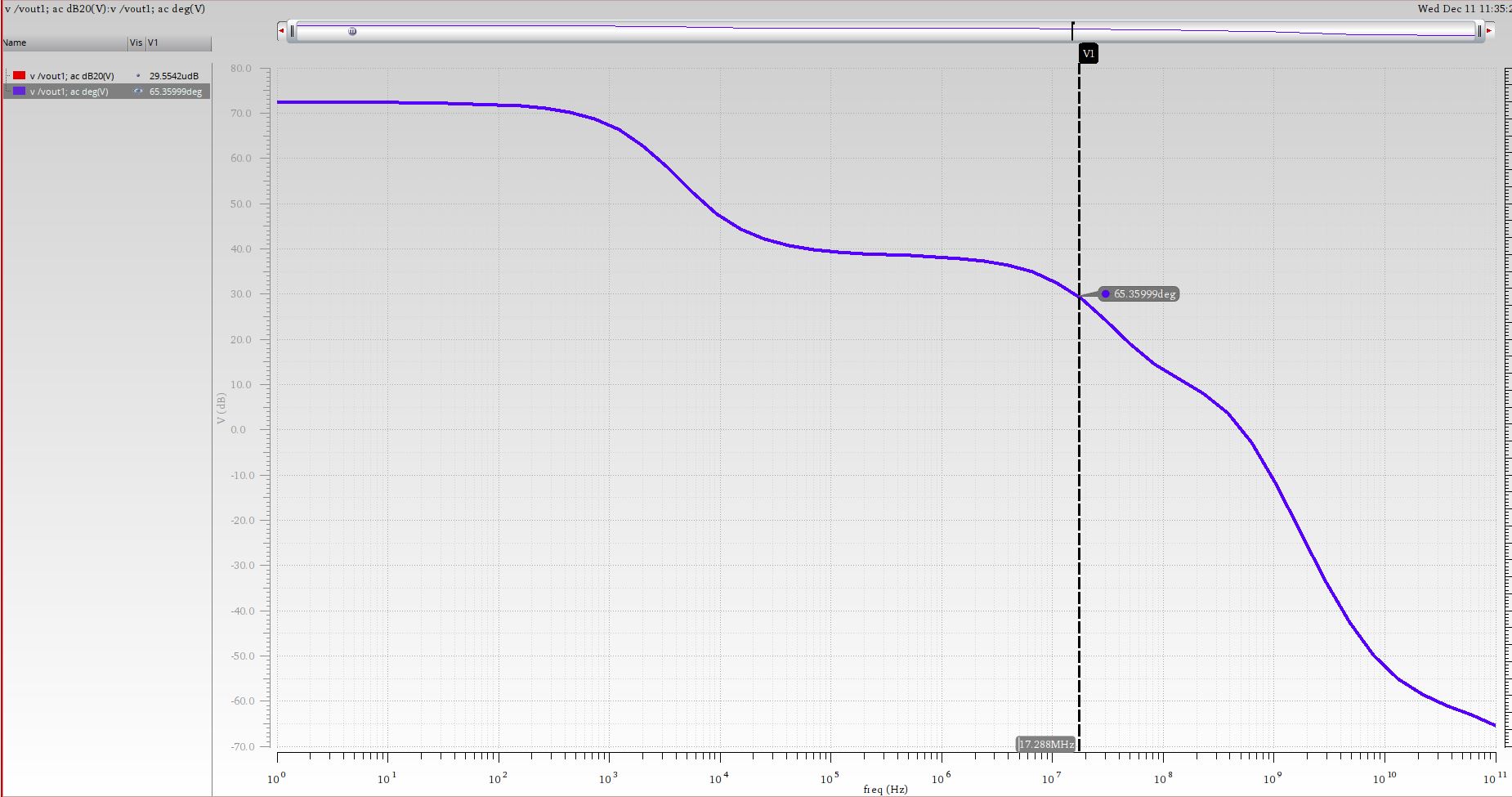
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**OUTPUTS**

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The gain simulated from the design is 73.1499 dB and the bandwidth is 17.288 MHz

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The phase margin simulated from the design is 65.35999°. The compensation capacitor has shifted the second pole further from the 3db frequency and almost nullified its effect on the gain and phase margin improving its performance by increasing the phase margin and hence a stability.

**RESULTS**

|  |  |  |
| --- | --- | --- |
| **Specifications** | **Given** | **Project Outputs** |
| Open loop gain | ≥ 65 dB | 73.1499 dB |
| Phase Margin | ≥60° | 65.35999° |
| Unity Gain Frequency | ≥ 15 MHz | 17.288 MHz |

Besides the results in the table above, we also have the following results from the analysis.

Gain (Calculated) = 73.03 dB

Gain (Simulated) = 73.14 dB

The simulated input common mode range is Vicmin = 210 mV and Vicmax = -700 mV. The simulated output common mode range is Vocmin = -212.629 mV and

Vocmax= 542.779mV. The transistors go out of saturation if the input goes beyond this range.